N2 Power System Architecture

Introduction

This technote provides information on the power system architecture of the N2 system. This note also provides data that was gathered on a single EVT2A system to check the performance of the power supply inside a working unit. The test data was taken at various system load conditions that may occur.

Power Architecture

Figure 1.0 shows the Power System Architecture of the N2 device. The Power System generates all the necessary voltages needed fot the Main Logic Board and associated Modules. As the diagram shows, each of the power supplies is controlled by an enable to turn on the supply.

Additionally, some device supplies in the system can be individually controlled even though the power supply is active.

1.7 Volt Supply

This section describes the operating characteristics of the 1.7 Volt Buck Regulator Power Supply. This supply powers the internal logic of the StrongArm CPU. A circuit diagram of the 1.7 volt supply is shown below and a table of the operating characteristics is provided.

Input Operating Range:
3.8V to 7.7V DC

Output	**Tolerance***	**Min Current**	**Max Current**	**Max Ripple/Noise**
+1.7Volts	±5%	0mA	200mA	15mV

* Regulation is maintained under all transient load conditions. Tolerence includes DC regulation plus ripple to 20MHz

Conditions

The 3.3 Volt supply operates in 4 load condition states. These states are Sleep, Idle, Run and Run plus powering a PCMCIA card.

The +5 Volt and the +12 Volt are used for FLASH writes, the Newton Interconnect line driver and by PCMCIA cards.

To simulate PCMCIA cards, testing was performed by adding external loads to simulate actual usage. The load used in this test was a 100mA constant current load for the +5 Volt power supply. This load was chosen instead of the maximum specified load of 500mA because at that maximum load, the supply operates in a continuous current condition, and output ripple decreases.

Testing was also performed with no external loads to capture data from the +12 Volt power supply performance during writes to internal flash and from the +5 Volt supply when powering the serial port.

The Variable LCD contrast output voltage was set to a typical condition with the system operating in run and rest mode.

During all these tests, the battery input voltage was held constant at +5 Volts.

Results

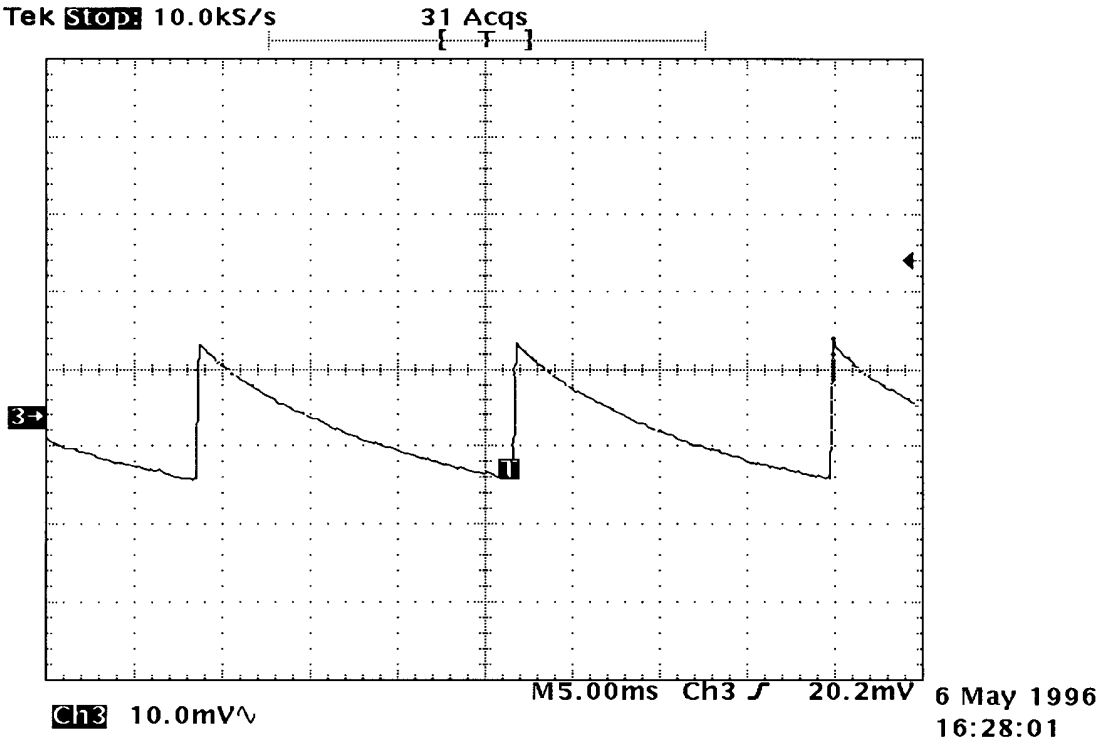
Input Voltage 5.0 Volts

	DC Output	Ripple PP mV	Ripple RMS mV	Ripple Frequency
3.3 Volt Supply				
Sleep	3.27	56	8	52Hz
Run mode	3.28	50	14	16.8kHz
Idle Mode	3.28	53	13	10.3kHz
Run +External Load (100mA)	3.28	42	13	34.25kHz
5 Volt Supply				
No External Load	5.11	125	31	191Hz
External Load (100mA)	5.14	320	77	1.77kHz
12 Volt Supply				
No External Load	12.04	60	11	204Hz
External Load (60mA)	12.09	60	16	25.7KHz
Variable LCD Bias Voltage				
Mixed Mode	24.11	46	13	8.6KHz

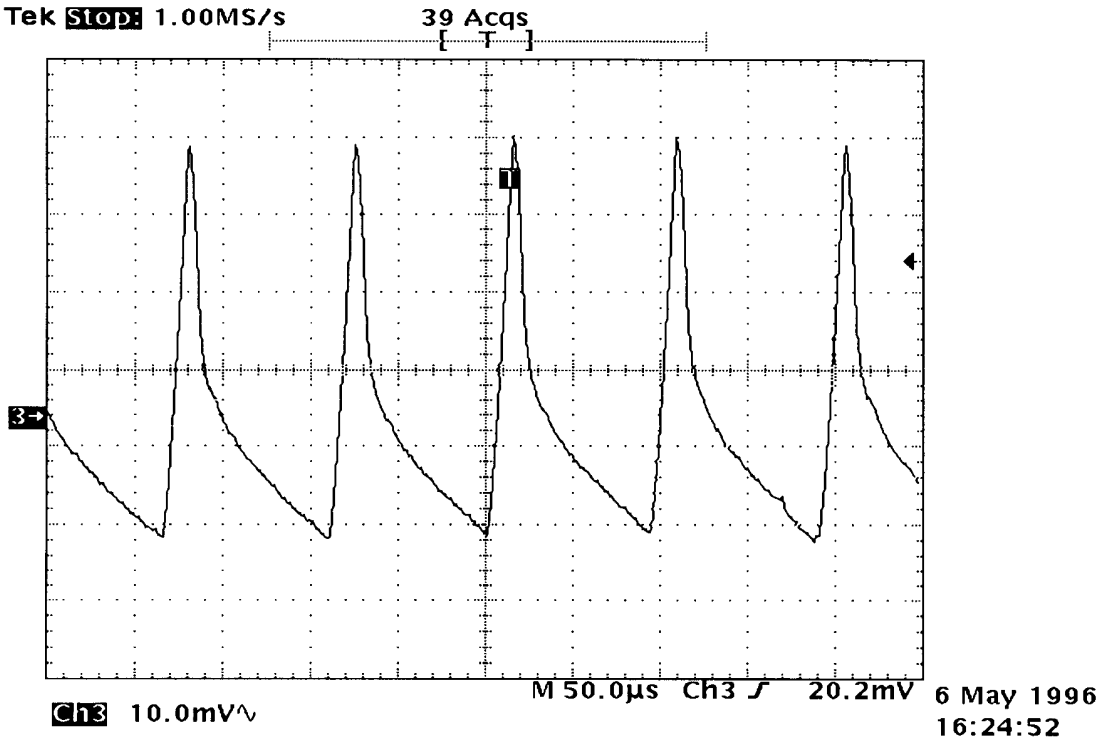
Pictures of Ripple waveforms

3.3V Output

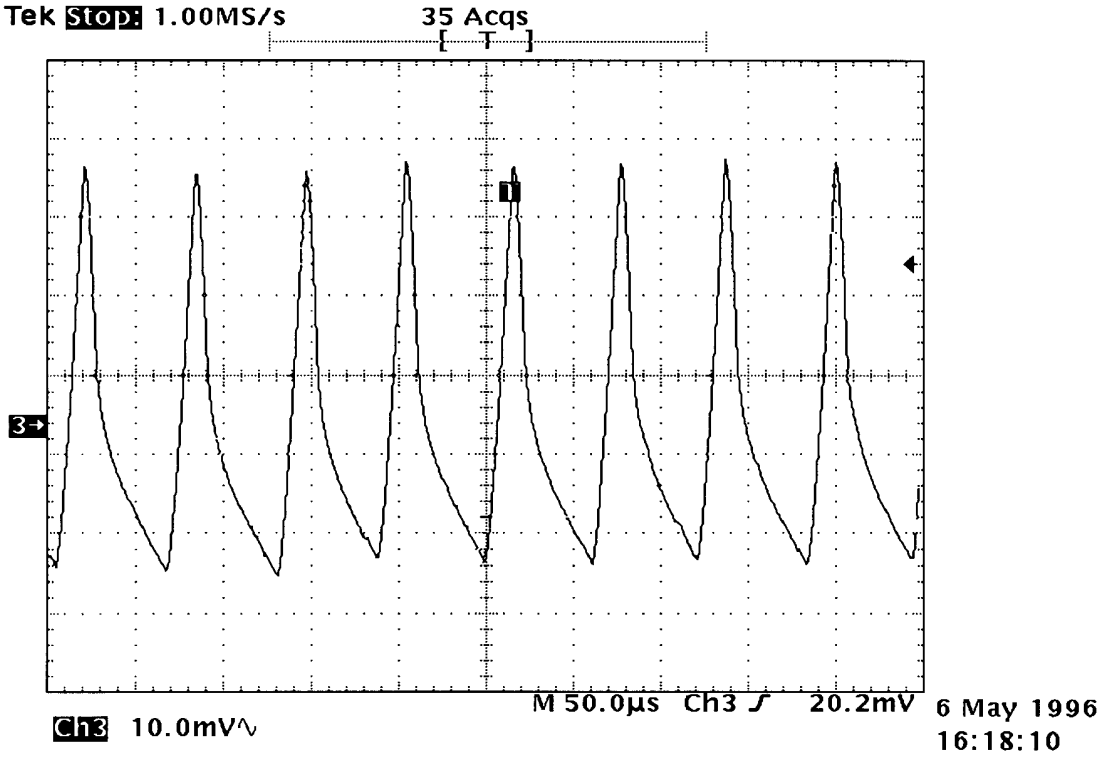
3.3V Ripple in Sleep Mode 10mV/Div



3.3V Output Ripple in Idle Mode 10mV/Div

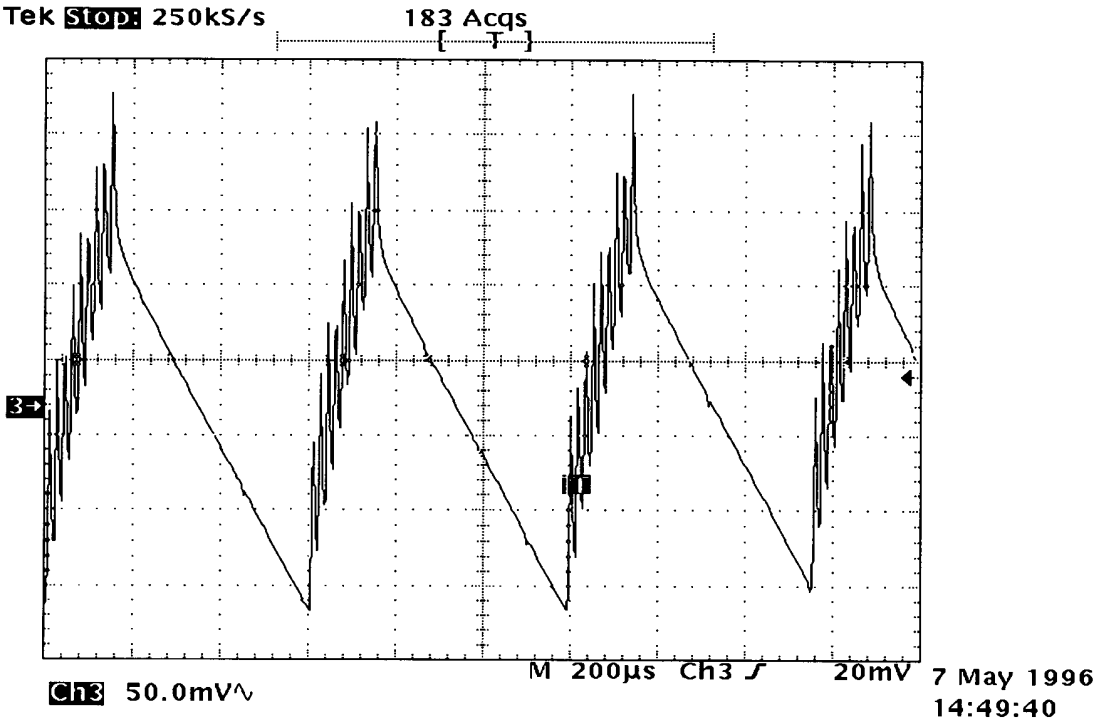


3.3V Ouput Ripple Run Mode 10mV/Div

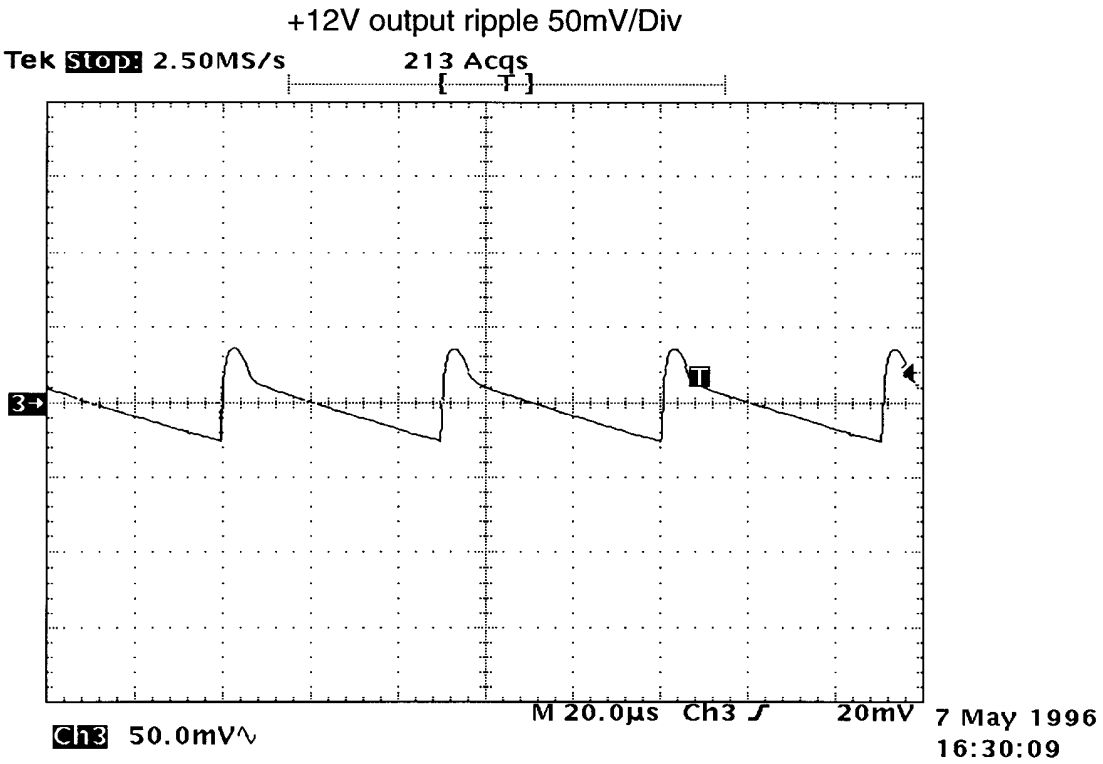


+5V Output

+5V Output with external load of 100mA- 50mV/Div



+12V Output


+12V output ripple 50mV/Div
Tek Stop: 2.50MS/s
213 Acqs
M 20.0µs Ch3 ƒ 20mV
Ch3 50.0mV
7 May 1996
16:30:09

LCD Bias Output